AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A circuit having a class-AB output stage, comprising: first, second, third, and fourth MOS transistor devices configured in a translinear loop including semiconductor junctions of the first, second, third, and fourth MOS transistor devices connected in series, semiconductor junctions of a first pair of the first, second, third, and fourth MOS transistor devices connected in a clockwise direction, and semiconductor junctions of a second different pair of the first, second, third, and fourth MOS transistor devices connected in a counter-clockwise direction, the first MOS transistor device carrying a first control current, the second MOS transistor device carrying a second control current, the third MOS transistor device carrying a current equal to the sum of the first and second control currents, and the fourth MOS transistor device carrying a bias current;

a first output circuit coupled to a first voltage supply and an output node, the first output circuit sourcing a first output current based on the first control current; and

a second output circuit coupled to a second voltage supply and the output node, the second output circuit sourcing a second output current based on the second control currents.

2. (Original) The circuit of claim 1 wherein the first and second output circuits are current mirrors and the first and second output currents equal the first and second control currents, respectively.

3. (Currently Amended) The circuit of claim 1 wherein the MOS transistor devices are NMOS devices.

4. (Currently Amended) The circuit of claim 1 wherein the MOS transistor devices operate in weak inversion mode.

5. (Original) The circuit of claim 1, further comprising a supply voltage having a voltage lower than 2 * VGS + VDSsat to provide the first voltage supply.

6. (Original) The circuit of claim 1, further comprising a supply voltage having a

voltage equal to VGS + 2* VDSsat to provide the first voltage supply.

7. (Original) The circuit of claim 1 wherein the bias current is programmable to permit user selection of a bias current.

8. (Original) The circuit of claim 1 wherein a quiescent current of the output stage is set by the bias control current, the bias current being increased above a selected predetermined level to lower a distortion level of the circuit.

9. (Original) The circuit of claim 8, further comprising an audio circuit wherein the output node is coupled to the audio circuit.

10. (Currently Amended) A circuit having a class-AB output stage, comprising:

a plurality of MOS transistor devices configured in a translinear loop to generate first and second control currents having a harmonic mean relationship, the translinear loop including an even number of semiconductor junctions of the plurality of MOS transistor devices connected in series, semiconductor junctions of a first even number of the plurality of MOS transistor devices connected in a clockwise direction, and semiconductor junctions of a second different even number of the plurality of MOS transistor devices connected in a counter-clockwise direction;

a first output circuit coupled to a first voltage supply and an output node, the first output circuit sourcing a first output current based on the first control current; and

a second output circuit coupled to a second voltage supply and the output node, the second output circuit sourcing a second output current based on the second control currents.

11. (Original) The circuit of claim 10 wherein the first and second output circuits are current mirrors and the first and second output currents equal the first and second control currents, respectively.

12. (Original) The circuit of claim 10 wherein the MOS transistor devices are NMOS devices.

13. (Currently Amended) The circuit of claim 10 wherein the MOS transistor devices operate in weak inversion mode.

14. (Original) The circuit of claim 10, further comprising a supply voltage having a voltage lower than 2 * VGS + VDSsat to provide the first voltage supply.

15. (Original) The circuit of claim 10, further comprising a supply voltage having a voltage equal to VGS + 2* VDSsat to provide the first voltage supply.

16. (Original) The circuit of claim 10 wherein the first voltage supply is 1.8 volts and the second voltage supply is a ground reference.

17. (Currently Amended) The circuit of claim 10 wherein the first and second output circuits comprise first and second output MOS transistor devices, respectively, the maximum output voltage range at the output node being substantially equal to the difference between the first and second voltage supplies minus a saturation voltage of the first and second MOS output transistor devices.

18. (Currently Amended) The circuit of claim 10 wherein the plurality of MOS transistor devices comprise first, second, third and fourth MOS transistor devices, wherein the first MOS transistor device is coupled to the first control current, the second MOS transistor device is coupled to a current that equals in the sum of the first and second control currents, the third MOS transistor device is coupled to the second control current, and a forth MOS transistor device is coupled to a bias control current.

19. (Currently Amended) The circuit of claim 18 wherein the sources of the second and third and MOS transistor devices are coupled to a bias voltage.

20. (Original) The circuit of claim 10 wherein a quiescent current of the output stage is set by a bias control current.

21. (Original) The circuit of claim 20, further comprising an audio circuit wherein the bias current is increased above a selected predetermined level to lower a distortion level of the circuit for use with the audio circuit.

22. (Original) The circuit of claim 20, further comprising a power control circuit wherein the output node is coupled to the power control circuit.

23. (New) The circuit of claim 1, further comprising:

a gate of the first MOS transistor device coupled to a gate of the third MOS transistor device to connect gate – source semiconductor junctions of the first and the third MOS transistor devices in series; and

a gate of the second MOS transistor device coupled to a gate of the fourth MOS transistor device to connect gate – source semiconductor junctions of the second and the fourth MOS transistor devices in series.

24. (New) The circuit of claim 23, further comprising:

a source of the first MOS transistor device coupled to a source of the fourth MOS transistor device to connect gate – source semiconductor junctions of the first and the fourth MOS transistor devices in series, and

a source of the second MOS transistor device coupled to a source of the third MOS transistor device to connect gate – source semiconductor junctions of the second and the third MOS transistor devices in series.

25. (New) The circuit of claim 24, further comprising:

a drain of the third MOS transistor device coupled to the gate of the third MOS transistor device and the gate of the first MOS transistor device; and

a drain of the fourth MOS transistor device coupled to the gate of the fourth MOS transistor device and the gate of the second MOS transistor device.

26. (New) The circuit of claim 25, further comprising:

a fifth MOS transistor device having a drain coupled to the source of the first MOS transistor device and the source of the fourth MOS transistor device to permit

the circuit to be modulated according to an input voltage applied to a gate of the fifth MOS transistor device; and

a bias voltage applied to the source of the second MOS transistor device and the source of the third MOS transistor device to provide a sink for the second control current carried by the second MOS transistor device and for the sum of the first and second control currents carried by the third MOS transistor device.

27. (New) The circuit of claim 10, wherein the plurality of MOS transistor devices comprise first, second, third and fourth MOS transistor devices, the circuit further comprising:

a gate of the first MOS transistor device coupled to a gate of the third MOS transistor device to connect gate – source semiconductor junctions of the first and the third MOS transistor devices in series; and

a gate of the second MOS transistor device coupled to a gate of the fourth MOS transistor device to connect gate – source semiconductor junctions of the second and the fourth MOS transistor devices in series.

28. (New) The circuit of claim 27, further comprising:

a source of the first MOS transistor device coupled to a source of the fourth MOS transistor device to connect gate – source semiconductor junctions of the first and the fourth MOS transistor devices in series, and

a source of the second MOS transistor device coupled to a source of the third MOS transistor device to connect gate – source semiconductor junctions of the second and the third MOS transistor devices in series.

29. (New) The circuit of claim 28, further comprising:

a drain of the third MOS transistor device coupled to the gate of the third MOS transistor device and the gate of the first MOS transistor device; and

a drain of the fourth MOS transistor device coupled to the gate of the fourth MOS transistor device and the gate of the second MOS transistor device.

30. (New) The circuit of claim 29, further comprising:

a fifth MOS transistor device having a drain coupled to the source of the first MOS transistor device and the source of the fourth MOS transistor device to permit the circuit to be modulated according to an input voltage applied to a gate of the fifth MOS transistor device; and

a bias voltage applied to the source of the second MOS transistor device and the source of the third MOS transistor device to provide a sink for the second control current carried by the second MOS transistor device and for the sum of the first and second control currents carried by the third MOS transistor device.